HIGH-EFFICIENCY, SMALL-CHIP AlGaAs/GaAs POWER HBTS FOR LOW-VOLTAGE DIGITAL CELLULAR PHONES

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ABSTRACT

A 61% power added efficiency (PAE), high linearity AlGaAs/GaAs power HBT with a very small chip size of 0.580.77 mm for use in personal digital cellular phones (PDC) is described. The device layout is optimized to reduce thermal resistance while maintaining a compact chip size. This power HBT, which has 60 fingers of 230m emitter, exhibited 31.4 dBm output power and 61% power added efficiency with -51.7 dBc adjacent channel leakage power at a 50 kHz offset frequency under 1.5 GHz/4-shifted QPSK modulation when operated at a low collector-emitter voltage of 3.4 V. These results satisfy Japan's PDC standard in a chip area that is less than 20% of that needed for a conventional GaAs power MESFET.

INTRODUCTION

With the rapid growth in cellular phone markets, there is an increasing demand for high performance power amplifiers that offer high power efficiency and linearity, with a low chip cost. For Personal Digital Cellular phone (PDC) applications, the currently available power amplifiers fabricated with GaAs FETs require a relatively large chip size because of the FET's large gate width, which is necessary to meet the requirement for output power above 30 dBm and adjacent channel leakage power (Padj) below -50 dBc at a 50 kHz offset frequency. As an alternative, AlGaAs/GaAs heterojunction bipolar transistors (HBTs) are considered excellent candidates for use as power devices, since they offer advantages over GaAs power FETs, such as their high power handling capability, which makes it possible to use a smaller chip area, and their ability to operate without a negative supply voltage. Several HBT power amplifiers for digital cellular phones have been reported (1)(2). However, the efficiency and linearity, as well as the chip size for the power amplifier were not attractive as compared with those of the power FET.

In this work, we have developed power AlGaAs/GaAs HBTs , with a device layout designed to be as compact as possible while achieving thermally stable operation in a multi-finger structure, and maintaining higher power added efficiency and lower adjacent channel leakage power.

THERMAL DESIGN

In practical power applications, the high power handling capabilities of HBTs are generally restrained by the thermal effect, due to the poor thermal conductivity of GaAs and thermally positive feedback of self-heating.

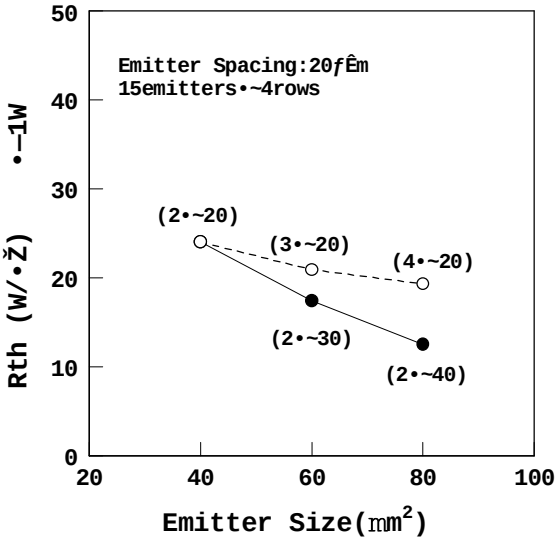

Fig. 1. Calculated thermal resistance *Rth* versus the emitter size for the 1 W power dissipation.

The device layout for a high-power HBT must be designed to ensure low and uniform junction temperatures. In our previous work, we used a three-dimensional thermal analysis that took into account the local-temperature dependence of the collector current to investigate the geometories of the emitter fingers and the

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chip. We have also determined the optimal chip thickness and emitter spacing for lower thermal resistance(3)(4).

In this work, the emitter size effect on the thermal properties is investigated with the goal of further reducing the thermal resistance. Figure 1 shows the calculated thermal resistance *Rth* versus the emitter size when 1 W DC power is applied to a multi-finger HBT arranged in four finger-rows of 15 emitters each, with 20 m emitter spacing on a 0.03 mm-thick chip.

Figure 1 clearly shows that the thermal resistance decreases as the emitter size increases, due to the heat source area being spread over on a chip area and the decreased dissipated power density. Comparing emitters of various shapes, a significant reduction in *Rth* is observed in the longer finger HBTs. This is thought to be due to an increase in the thermal cross-talk between the fingers in the wider emitter HBTs. The estimated thermal resistance was as small as 17/W for a 230 m emitter power HBT.

DEVICE FABRICATION

The power HBTs were fabricated using a self-alignment process on 3 inch-diameter MOCVD wafers. The epitaxial layer mainly consisted of a 220 nm-thick N-$Al_{0.25}Ga_{0.75}As$ graded($N=310^{17}cm^{-3}$) emitter layer, an 80 nm-thick p-GaAs ($p^{+}=410^{19}cm^{-3}$) uniform base layer, a 500 nm-thick n-GaAs($n=510^{16}cm^{-3}$) collector layer, and a 500 nm-thick n-GaAs($n=310^{18}cm^{-3}$) subcollector layer. Dopants for the n-type and p-type layers were Si and C, respectively.

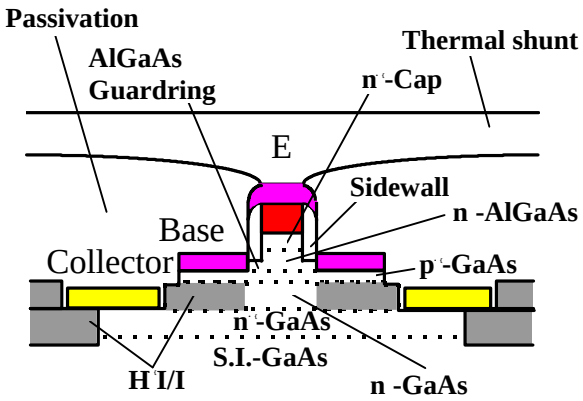

Fig. 2. Schematic cross-section of the self-aligned AlGaAs/GaAs HBT.

Figure 2 shows a cross-sectional view of the single finger emitter HBT. The detailed fabrication process steps have been described elsewhere(4). An AlGaAs guardring was formed at the emitter mesa periphery to reduce the base recombination current. The emitter, base and collector electrodes, respectively, consisted of WSi/Ti/Pt/Au, Pt/Ti/Pt/Au and Ni/AuGe/Au metal systems. The backside of the substrate was thinned to 30m and a 15m-thick Au plated heat sink was used to ensure low thermal resistance. Only twelve photo masks were needed for the entire fabrication process, including the backside processes. This is comparable to the number of masks needed in a typical power GaAs FET process.

As we previously reported, the chip surface temperature increases with a decreasing collector-emitter voltage under constant power dissipation, due to an increase in the amount of heat flowing from the heat source region (i.e. the collector depletion region) to the chip surface (4). This means that consideration of the chip surface temperature become important for low-voltage operation power HBTs. Thus, heat can be removed effectively through the emitter as well as through the wafer backside. Therefore, the thermal shunt emitter interconnection structure was adopted to make the junction temperature uniform.

A fabricated power HBT is shown in Fig. 3. Based on thermal design considerations, the emitters are arranged in four finger-rows of 15 emitters each, with 20 m emitter spacing on a 0.580.770.03 mm chip. The thermal shunt is plated with 3.0 m-thick Au.

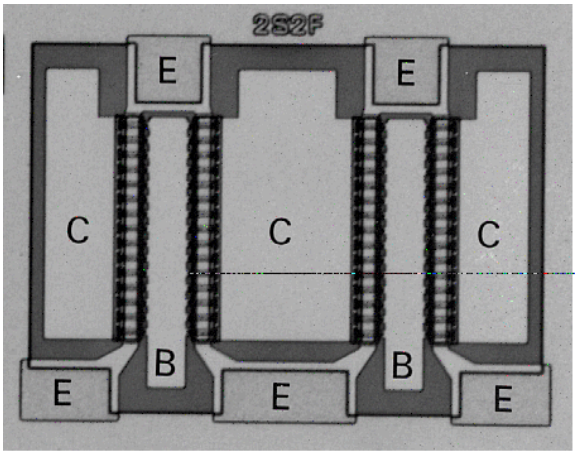

Fig. 3. Chip photograph of a fabricated power HBT constructed with four finger-rows of 15 emitters each (total 60 emitters) on a 0.580.770.03mm chip.

The fabricated HBT exhibited a typical current gainof 60, and a collector-emitter breakdown voltage BVceo of 12 V. The collector-emitter offset voltage was below 0.2 V. The current gain collapse phenomenon was not observed.

POWER PERFORMANCE

The 60 emitter HBT power amplifiers with various emitter sizes were examined the RF performance with a 1.5 GHz /4-shifted QPSK modulated signal for the PDC

system. The devices were examined at a low collector voltage of 3.4 V, which corresponds to the DC operating voltage for the PDC system where one Li-ion battery cell is used. The input and output matching circuits consisted of 50 microstrip lines connected with variable shunt capacitors.

Figure 4 shows comparisons of the PAE, associated gain, and Padj at a 50 kHz offset frequency for the power HBTs with various emitter sizes. All devices were operated under class AB conditions with a collector current of around 200 mA and a collector voltage of 3.4 V. Tuning was adjusted to minimize Padj at Pout of around 31.4 dBm, while keeping a maximum PAE. Although the associated gain decreased when the emitter size increased, the Padj improved while ensuring less than -50dBc. Thus, these devices satisfied the PDC standard in a chip area that is less than 20% of that needed for a conventional GaAs power MESFET(5). The highest PAE of above 61% was achieved in both the 230m, and 320m emitter HBTs.

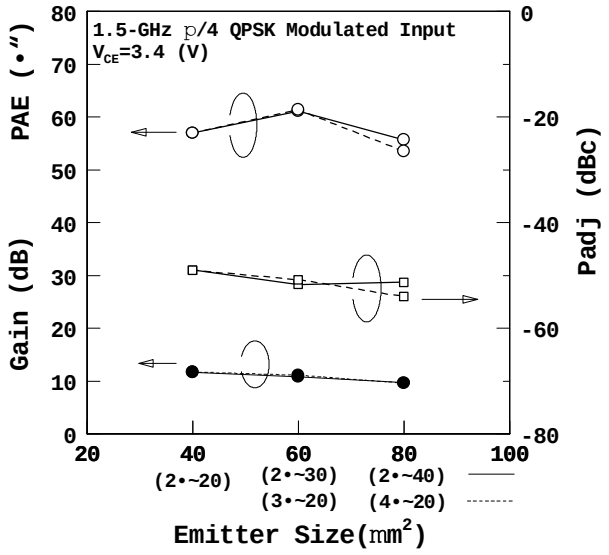

Fig. 4. Measured dependence of the power gain, power added efficiency, and adjacent channel leakage power on the emitter size (in a 60-emitter array) at Vce=3.4 V.

Figure 5 shows Pout, PAE, and Padj as a function of input power for the 230 m-emitter power HBT. The device was operated under class AB conditions with collector current of 200mA under fixed base-emitter voltage. The power HBT achieves less than -50dBc Padj as well as more than 30dBm Pout at 18.6dBm or more input power, which satisfy the PDC specification. A 31.4 dBm Pout, 61.1% PAE, and -51.7 dBc Padj with an associated gain of 10.8 dB was demonstrated at an input power of 20.6 dBm. To best of our knowledge, this is the highest PAE yet reported from an L-band GaAs power transistor for low-voltage digital cellular applications.

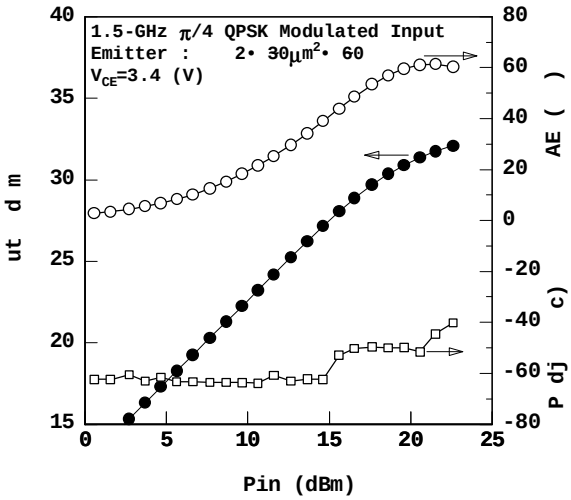

Fig. 5. Measured output power, power added efficiency, and adjacent channel leakage power at the 50 kHz offset frequency vs. input power at Vce=3.4 V for 230m60-emitter HBT.

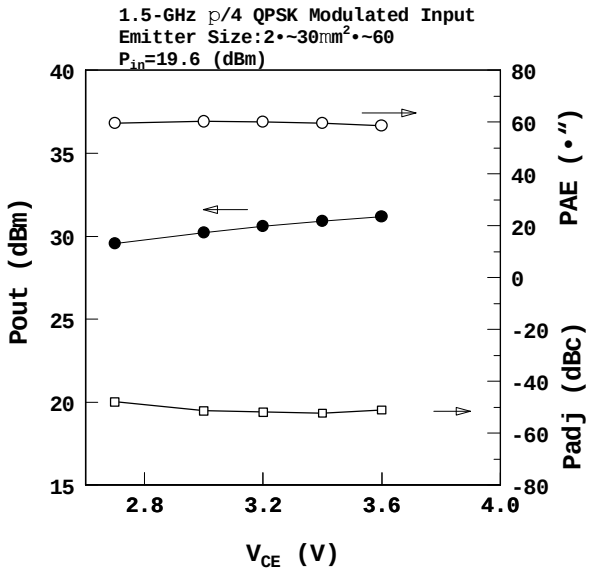

Fig. 6. Measured bias-dependent output power, power added efficiency, and adjacent channel leakage power for 60-emitter HBT. The input power and matching condition are fixed at Vce=3.4 V.

Figure 6 shows the dependence of Pout, PAE, and Padj on the operating voltage Vce for the 230m60-emitter power HBT. The input power, matching condition and base-emitter voltage are fixed at the optimized values for Vce=3.4V operation. As the collector-emitter voltage

decreased, Pout decreased slightly and Padj increased slightly, but the PAE remained steady at about 60%. Even at a low Vce of 2.7 V, the developed power HBT showed 29.6dBm Pout and 59.6% PAE with -48 dBc Padj. This performance will increase the battery-life in PDC systems.

CONCLUSION

We have developed a high efficiency, high linearity AlGaAs/GaAs power HBT with a very small chip size of 0.580.77 mm for use in personal digital cellular phones. The device layout is optimized to reduce thermal resistance while maintaining a compact chip size. The developed power HBT with 60 fingers of 230 m emitter exhibited 31.4 dBm output power and 61% power added efficiency with -51.7 dBc adjacent channel leakage power at a 50 kHz offset frequency under 1.5 GHz/4-shifted QPSK modulation when operated at a low collector-emitter voltage of 3.4 V. These results satisfy Japan's PDC standard in a chip area that is less than 20% of that needed for a conventional GaAs power MESFET. Also, this is the highest PAE of an L-band GaAs power transistor reported to date for low-voltage digital cellular applications.

These results demonstrate that the developed HBT is very suitable for compact low-cost personal digital cellular power-module applications that operate at low DC supply voltages.

ACKNOWLEDGMENTS

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